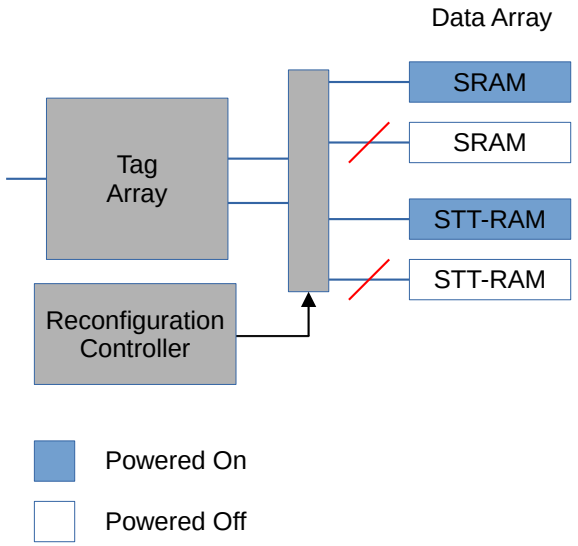
Investigating Dynamically Reconfigurable Hybrid Caches

Novel non-volatile memory technologies such as STT-RAM promise great potential when introduced at cache level. While achieving lower static power consumptions and requiring lower read currents than SRAM, they come with the drawback of an increased write overhead. Therefore, hybrid caches consisting of both volatile and non-volatile cache-lines are of great research interest. One possibility to balance these trade-offs is to dynamically reconfigure the cache by powering off parts of the cache currently not needed, reducing the static power consumption, while providing cache-lines in the technology best suited for the current access pattern can reduce the dynamic energy consumption.



This thesis thus aims to investigate whether dynamically reconfigurable hybrid caches can overcome their inherent overhead to help develop energy-efficient systems. For this purpose the system simulator gem5 (`gem5.org`) shall be used, and if necessary extended, to perform simulation-based evaluations of different reconfiguration techniques.

Prerequisites:	Knowledge in C/C++ and Python, basic knowledge about caches
Type of Work:	Theory (30%), concept (35%), implementation (35%)
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